REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendments and the following remarks.

The Applicants appreciate the acknowledgement of allowable subject matter in claim 5, and the allowance of claims 8-14.

By the foregoing amendment, claims 18-20 have been canceled, ands claims 2, 7 and 15 have been amended. Thus, claims 2-16 are pending in the application, with claims 2-4, 6, 7 and 15-16 subject to examination.

In the outstanding Office Action mailed November 7, 2005, claims 2-4, 6, 15, 16 and 18-20 were rejected under 35 USC § 103(a) as being unpatentable over U.S. Patent No. 6,590,422 to Dillon ("Dillon") in view of U.S. Patent No. 6,774,695 to Hayashi et al. ("Hayashi"), and claim 7 was rejected under 35 USC § 103(a) as being unpatentable over Dillon in view of Tinsley (US 2003/0085736). It is noted that claims 18-20 have been canceled, and claims 2, 7 and 15 have been amended. To the extent that the rejections remain applicable to the claims currently pending, the Applicants hereby traverse the rejections, as follows.

The Applicants submit that none of the cited references, nor combination thereof, discloses or suggests at least the combination of a differential amplification circuit, connected to the level conversion circuit, for functioning in accordance with the first and second output signals of the level conversion circuit and generating a differential amplification output signal, wherein the first and fourth MOS transistors each have a gate for receiving a first input signal, and the second and third MOS transistors each have a gate for receiving a second input signal having a phase inverted from the phase

of the first input signal, and wherein the gate of each transistor has a gate length and a gate width, the ratio between the gate length and the gate width of one of the transistors in each pair of the series-connected MOS transistors is about three times or less than the ratio between the gate length and the gate width of the other one of the transistors in the pair of the series-connected MOS transistors such that fluctuation of a voltage level of the differential amplification output signal is suppressed and fluctuation of delay time of the differential amplification output signal is in a predetermined time period regardless of a change in voltage levels of the first and second input signals, as recited in claims 2 and 15, as amended.

Hayashi only discloses setting the ratio between the gate width and the gate length of the first p-channel type MOS transistor (Qp5) to be greater than the ratio between the gate width and the gate length of the second p-channel type MOS transistor (Qp6) (e.g. 2:1), setting the ratio between the gate width and the gate length of the second n-channel type MOS transistor (Qn6) to be greater than the ratio between the gate width and the gate length of the first n-channel type MOS transistor (Qn5) (e.g. 2:1), thereby reducing the on-resistances of the first p-channel type MOS transistor (Qp5) and the second n-channel type MOS transistor (Qn6) which serve as resistive loads, contributing to further accelerating the variation of the output signal. Neither Hayashi nor Dillon discloses or suggests at least the combination of the ratio between the gate length and the gate width of one of the transistors in each pair of the series connected MOS transistors is about three times or less than the ratio between the gate length and the gate width of the other one of the transistors in the pair of the series connected MOS transistors such that fluctuation of a voltage level of the differential

amplification output signal (e.g., X) is suppressed and fluctuation of delay time (e.g., tPD) of the differential amplification output signal is in a predetermined time period (e.g. 75ps), regardless of a change in voltage levels of the first and second input signals (e.g., IN, INB) as recited in claims 1 and 15, as amended.

For at least this reason, the Applicants submit that claims 2 and 15, as amended, are allowable over the cited art of record. As claims 2 and 15 are allowable, the Applicants submit that claims 3-7 and 16, which depend from allowable claims 2 and 15, respectively, are likewise allowable.

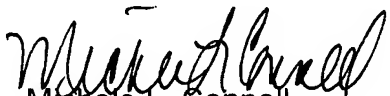
Conclusion

For all of the above reasons, it is respectfully submitted that the claims now pending patentability distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is requested to contact the undersigned representative at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The fee for this extension may be charged to our Deposit Account No. 01-2300. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300, referencing docket no. 108075-00126.

Respectfully submitted,



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